What is claimed is:

1. A semiconductor device comprising:

a memory cell array connected to one of a plurality of wordlines and a plurality of bitline pairs;

a sense amplifier amplifying data read from the memory cell array;

a control circuit controlling writing/reading of data to/from the memory cell array;

a row decoder decoding an address signal and outputting a decoded signal to select one of the plurality of wordlines;

a bitline-pair voltage setting circuit setting a voltage of at least one of the plurality of bitline pairs to a bitline test voltage in a test mode; and

a wordline driver setting the low-level voltages of the plurality of wordlines to a wordline test voltage in the test mode,

wherein the wordline test voltage can be set to be different from the low-level voltage of the plurality of wordlines in a normal operation mode.

2. The semiconductor device of claim 1, wherein the low-level voltage of the wordlines in the normal operation mode is a ground voltage.

3. The semiconductor device of claim 2, further comprising a wordline test voltage terminal receiving the wordline test voltage, wherein the wordline test voltage terminal is separate from a ground voltage terminal, which receives the ground voltage.

4. The semiconductor device of claim 3, further comprising:

a ground voltage connection unit connected to the ground voltage terminal; and

a wordline test voltage connection unit connected to the wordline test voltage terminal.

5. The semiconductor device of claim 3, further comprising a ground voltage connection unit connected to the ground voltage terminal and the wordline test voltage terminal upon packaging of the semiconductor device.

6. The semiconductor device of claim 1, wherein the wordline driver comprises:

an odd wordline driver connected to an odd wordline; and

an even wordline driver connected to an even wordline,

wherein the odd wordline driver and the even wordline driver can independently set the low-level voltages of the odd wordline and the even wordline, respectively, in the test mode.

7. The semiconductor device of claim 6, wherein the odd wordline alternates with the even wordline.

8. The semiconductor device of claim 1, wherein the memory cell array comprises:

a plurality of memory cells, wherein each memory cell is connected to one of the plurality of wordlines and the plurality of bitline pairs.

9. A semiconductor device comprising:

a memory cell array including a plurality of memory cells, each memory cell connected to one of a plurality of wordlines and a plurality of bitline pairs;

a row decoder decoding an address signal and outputs a decoded signal to select one of the plurality of wordlines;

an odd wordline driver setting low-level voltages of an odd wordline to an odd low-level voltage in a test mode; and

an even wordline driver setting the low-level voltages of even wordlines to an even low-level voltage in the test mode,

wherein both the odd low-level voltage and the even low-level voltage can be set to be different from the low-level voltages of the plurality of wordlines set in a normal operation mode.

10. The semiconductor device of claim 9, further comprising a bitline pair voltage setting circuit, which sets the voltage of at least one of the plurality of bitline pairs to a bitline test voltage level.

11. The semiconductor device of claim 9, wherein the odd wordlines alternate with the even wordlines.

12. The semiconductor device of claim 9, further comprising:

an odd low-level voltage terminal receiving the odd low-level voltage; and

an even low-level voltage terminal receiving the even low-level voltage, wherein the odd low-level voltage terminal and the even low-level voltage terminal are separate from a ground voltage terminal, which receives the ground voltage.

13. The semiconductor device of claim 12, further comprising:

a ground voltage connection unit connected to the ground voltage terminal;

an odd low-level voltage connection unit connected to the odd low-level voltage terminal; and

an even low-level voltage connection unit connected to the even low-level voltage terminal.

14. The semiconductor device of claim 12, further comprising a ground voltage connection unit connected to the ground voltage terminal, the odd low-level voltage terminal, and the even low-level voltage terminal upon packaging of the semiconductor device.

15. The semiconductor device of claim 9, wherein the semiconductor device is a static random access memory (SRAM).

16. A method of testing a semiconductor device, which comprises memory cells, each memory cell connected to one of a plurality of wordlines and a plurality of bitline pairs, the method comprising:

writing test data to the memory cells;

setting the low-level voltage of the plurality of wordlines to a wordline test voltage;

setting the voltage of at least one of the plurality of bitline pairs to a true test voltage and a complementary test voltage;

wherein the plurality of wordlines, stand by in an activated state for a period of time;

reading data from the memory cells; and

comparing the read data with the written test data,

wherein the wordline test voltage can be set independently of the low-level voltage of the plurality of wordlines set in a normal operation mode.

17. The method of claim 16, wherein the test data is 0 or 1.

18. The method of claim 17, wherein the test data writing step comprises:

activating the plurality of wordlines at the same time by adjusting the wordline test voltage; and

simultaneously writing the test data to memory cells connected to the activated wordlines.

19. The method of claim 16, further comprising classifying the plurality of wordlines into odd wordlines and even wordlines,

wherein the low-level voltage of the odd wordlines can be adjusted independently of the low-level voltage of the even wordlines.

20. The method of claim 19, wherein in the test data writing step, data written to memory cells connected to the odd wordlines differs from the data written to memory cells connected to the even wordlines.

21. The method of claim 19, wherein the test data writing step comprises:

activating the plurality of odd wordlines at the same time by adjusting the low-level voltage of the odd wordlines;

simultaneously writing the test data to memory cells connected to the odd wordlines;

activating the plurality of even wordlines at the same time by adjusting the low-level voltage of the even wordlines; and

simultaneously writing the test data to memory cells connected to the even wordlines.

22. A method of testing a semiconductor device, which comprises memory cells, each memory cell connected to one of a plurality of wordlines and a pair of a plurality of bitline pairs, the method comprising:

writing test data to the memory cells;

setting the low-level voltage of the plurality of wordlines to a wordline test voltage;

selecting one of the plurality of wordlines and activating the selected wordline;

writing data opposite to the test data to memory cells connected to the selected wordline, for a period of time;

reading data from the memory cells other than the memory cells containing the data; and

comparing the read data with the written test data,

wherein the wordline test voltage can be set independently of the low-level voltage of the plurality of wordlines set in a normal operation mode.

23. The method of claim 22, wherein the test data is 0 or 1.

24. The method of claim 22, wherein the test data writing step comprises:

activating the plurality of wordlines at the same time by adjusting the wordline test voltage; and

simultaneously writing the test data to memory cells connected to the activated wordlines.

25. The method of claim 22, further comprising classifying the plurality of wordlines into odd wordlines and even wordlines,

wherein the low-level voltage of the odd wordlines can be adjusted independently of the low-level voltage of the even wordlines.

26. The method of claim 25, wherein the test data writing step comprises:

activating the plurality of odd wordlines at the same time by adjusting the low-level voltage of the odd wordlines;

simultaneously writing the test data to memory cells connected to the odd wordlines;

activating the plurality of even wordlines at the same time by adjusting the low-level voltage of the even wordlines; and

simultaneously writing the test data to memory cells connected to the even wordlines.